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EXAMINER	
RAINEY, ROBERT R	

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2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/705,775	MAEDA ET AL.	
	Examiner	Art Unit	
	Robert R. Rainey	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003 and 08 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1, 2, 3, 4, 7, 10, 11, 12, 15, 18, 19, and 21** are rejected under 35 U.S.C. 102(b) as being anticipated by Japanese Patent Application No. *JP2000-181394* ("*Sunao*").

Regarding **Claim 1**, *Sunao* teaches a data signal line driving method for driving a plurality of data signal lines ("S1-S4n" in Fig 1 and paragraph 0025) respectively so as to fetch (Fig 1 sampling circuit 130, switch 131, decoder 140 and sampling signals X1...X4 with operation described in Figs 4-7, 9 and 10) a multiphased video signal ("V1-Vn" in Figs 4-7, 9, and 10) via a plurality of video signal lines ("V1-Vn" in Fig 1 and paragraph 0025) into the data signal lines, said method comprising the steps of: gathering data signal line groups (all n data signal line groups are "gathered" that is treated as a single block as shown in Figs 4-7, 9, and 10), each made up of a predetermined number of the data signal lines sequentially connected to each of the video signal lines (4 data signal lines, i.e. S1-S4 to V1, S4-S8 to V2, ... S4(n-3)-S4(n) to Vn, are shown sequentially

connected to each video signal line in Fig 1), whose number is the same as the number of the video signal lines (Fig 1 shows n video signal lines and n groups of data lines), said data signal line groups being regarded as a single block (data signal line groups 1-n are "gathered" that is treated as a single block as shown in Figs 4-7, 9, and 10); and fetching the video signal from the video signal lines into the data signal lines in each block (see Figs 4-7, 9, and 10).

Regarding **Claim 2**, *Sunao* teaches a data signal line driving method for driving a plurality of data signal lines (see Fig 12) respectively so as to (i) multiphase a video signal having a plurality of color signals (VG1,VB1,VR1 ... of Fig 12) and (ii) fetch the video signal into the data signal lines, said method comprising the steps of: causing a plurality of divisional video signal lines, divided so as to respectively correspond to the color signals, to constitute each of the video signal lines ("V1-Vn" in Fig 1 and paragraph 0025 as modified by Fig 12 and paragraph 0101) ; gathering data signal line groups (all n data signal line groups are "gathered" that is treated as a single block as shown in Figs 4-7, 9, and 10), each made up of a predetermined number of the data signal lines sequentially connected to each of the divisional video signal lines so as to respectively correspond to the color signals (4 data signal lines, i.e. S1-S4 to V1, S4-S8 to V2, ... S4(n-3)-S4(n) to Vn, are shown sequentially connected to each video signal line in Fig 1 and Fig 12 and paragraph 0101 extend this to color signals), whose number is the same as the number of the video signal lines (Fig

1 shows n video signal lines and n groups of data lines. Fig 12 and paragraph 0101 extend this to color), said data signal line group being regarded as a single block (data signal line groups 1-n are "gathered" that is treated as a single block as shown in Figs 4-7, 9, and 10 and Fig 12 and paragraph 0101 extend this to color); and fetching the video signal from the video signal lines into the data signal lines in each block (Fig 1 sampling circuit 130, switch 131, decoder 140 and sampling signals X1...X4 with operation described in Figs 4-7, 9 and 10 expanded to color by Fig 12 and paragraph 0101).

Regarding **Claim 3**, *Sunao* teaches a data signal line driving circuit, which drives a plurality of data signal lines ("S1-S4n" in Fig 1 and paragraph 0025) respectively so as to fetch (Fig 1 sampling circuit 130, switch 131, decoder 140 and sampling signals X1...X4 with operation described in Figs 4-7, 9) a multiphased video signal ("V1-Vn" in Figs 4-7, 9, and 10) via a plurality of video signal lines ("V1-Vn" in Fig 1 and paragraph 0025) into the data signal lines, comprising: data signal line groups (Fig 1 and paragraph 0028), each made up of a predetermined number of the data signal lines sequentially connected to each of the video signal lines (4 data signal lines, i.e. S1-S4 to V1, S4-S8 to V2, ... S4(n-3)-S4(n) to Vn, are shown sequentially connected to each video signal line in Fig 1); and a video signal fetching section (Fig 1 sampling circuit 130, switch 131, decoder 140 and sampling signals X1...X4) for fetching the video signal from the video signal lines into the data signal lines in each block when gathering

data signal line groups (all n data signal line groups are "gathered" that is treated as a single block as shown in Figs 4-7, 9, and 10), each made up of a predetermined number of the data signal lines sequentially connected to each of the video signal lines (4 lines, i.e. S1-S4 to V1, S4-S8 to V2, ... S4(n-3)-S4(n) to Vn, are shown sequentially connected to each video signal line in Fig 1), whose number is the same as the number of the video signal lines (Fig 1 shows n video signal lines and n groups of data lines), said data signal line groups being regarded as a single block (data signal line groups 1-n are "gathered" that is treated as a single block as shown in Figs 4-7, 9, and 10).

Regarding **Claim 4**, *Sunao* teaches the data signal line driving circuit as set forth in claim 3, wherein the video signal fetching section includes drive switching means (Fig 1 decoder 140 and associated sampling signals X1, X2, X3, X4) for switching between (i) first driving in which each of the data signal lines of one of the data signal line groups in the block and each of the data signal lines of another one of the data signal line groups in the block are driven at the same time and (ii) second driving in which all the data signal lines of the data signal line groups are driven at the same time (Fig 1 decoder 140 and sampling signals X1, X2, X3, X4 allow any combination of the four sampling switches 131 in each data signal line group to sample the group's respective video signal clearly covering one per data signal line group and all signal lines in the signal

line groups. Fig 4 illustrates one data signal line per group at a time sampling and Fig 6 illustrates all signal lines in the groups sampling at the same time).

Regarding **Claims 7, 12, and 15**: these claims parallel Claim 4, substituting in the case of claims 7 and 15 the word "circuit" for "means", and are rejected by the same argument; see rejection of Claim 4 above.

Regarding **Claim 10**, *Sunao* teaches the data signal line driving circuit as set forth in claim 3, and further teaches that the data signal line groups are data signal line sets each of which is made up of a predetermined number of data signal lines respectively corresponding to color signals contained in the video signal fetched into the data signal lines (Fig 1 and paragraph 0028 as extended to color by Fig 12 and paragraph 0101).

Regarding **Claim 11**, *Sunao* teaches a data signal line driving circuit, which drives a plurality of data signal lines (see Fig 12) respectively so as to (i) multiphase a video signal having a plurality of color signals (VG1,VB1,VR1 ... of Fig 12) and (ii) fetch the video signal into the data signal lines, comprising: a plurality of divisional video signal lines, divided so as to respectively correspond to the color signals, which constitute each of the video signal lines ("V1-Vn" in Fig 1 and paragraph 0025 as modified by Fig 12 and paragraph 0101); and a video signal fetching section (Fig 1 sampling circuit 130, switch 131, decoder 140 and

sampling signals X1...X4 with operation described in Figs 4-7, 9 and 10 expanded to color by Fig 12 and paragraph 0101) for fetching the video signal from the video signal lines into the data signal lines in each block when gathering data signal line groups (all n data signal line groups are "gathered" that is treated as a single block as shown in Figs 4-7, 9, and 10), each made up of a predetermined number of the data signal lines sequentially connected to each of the divisional video signal lines so as to respectively correspond to the color signals (4 data signal lines, i.e. S1-S4 to V1, S4-S8 to V2, ... S4(n-3)-S4(n) to Vn, are shown sequentially connected to each video signal line in Fig 1 and Fig 12 and paragraph 0101 extend this to color signals), whose number is the same as the number of the video signal lines (Fig 1 shows n video signal lines and n groups of data lines. Fig 12 and paragraph 0101 extend this to color), said data signal line group being regarded as a single block (data signal line groups 1-n are "gathered" that is treated as a single block as shown in Figs 4-7, 9, and 10 and Fig 12 and paragraph 0101 extend this to color).

Regarding **Claims 12 and 15**: Claims 12 and 15 (15 assumed to depend from Claim 11) parallel Claim 4 and are reject by the same argument; see rejection of Claim 4 above. (Since there may be some claim dependency issues: note that the dependency of Claim 12 or 15 from Claim 11 or 2 does not change the argument for rejection.)

Regarding **Claim 18**,*Sunao* teaches the data signal line driving circuit as set forth in claim 11, and further teaches that the data signal line groups are data signal line sets each of which is made up of a predetermined number of data signal lines respectively corresponding to color signals contained in the video signal fetched into the data signal lines (Fig 1 and paragraph 0028 as extended to color by Fig 12 and paragraph 0101).

Regarding **Claim 19**, *Sunao* teaches a display device, comprising: a display panel (paragraph 0105 and Figs. 13 and 14) which includes (i) a plurality of data signal lines ("S1-S4n" in Fig 1 and paragraph 0025), (ii) a plurality of scanning signal lines provided so as to cross the data signal lines (G1 to Gm in Fig 1 and paragraph 25), and (iii) pixels provided on intersections of the data signal lines and the scanning signal lines (118 in Fig 1 and paragraph 0025), a video signal for displaying an image being fetched from the data signal lines into the pixels in synchronism with a scanning signal supplied from the scanning signal lines (Figs. 1 and 4 and paragraph 0033), said video signal being retained (paragraph 0036 describes "a picture signal...written in a pixel"); a data signal line driving circuit for outputting the video signal to the data signal lines in synchronism with a predetermined timing signal (Figs. 1 and 4 and paragraph 0036); and a scanning signal line driving circuit for outputting the scanning signal to the scanning signal lines in synchronism with a predetermined timing signal (Figs. 1 and 4 and paragraph 0033), said video signal being multiphased ("V1-

Vn" in Figs 4-7, 9, and 10), and being supplied to the data signal lines via a plurality of video signal lines ("V1-Vn" in Fig 1 and paragraph 0025), wherein the data signal line driving circuit, which drives said plurality of data signal lines respectively so as to fetch the multiphased video signal via said plurality of video signal lines into the data signal lines, includes: data signal line groups (Fig 1 and paragraph 0028), each made up of a predetermined number of the data signal lines sequentially connected to each of the video signal lines (4 data signal lines, i.e. S1-S4 to V1, S4-S8 to V2, ... S4(n-3)-S4(n) to Vn, are shown sequentially connected to each video signal line in Fig 1); and a video signal fetching section (Fig 1 sampling circuit 130, switch 131, decoder 140 and sampling signals X1...X4) for fetching the video signal from the video signal lines into the data signal lines in each block when gathering data signal line groups (all n data signal line groups are "gathered" that is treated as a single block as shown in Figs 4-7, 9, and 10), each made up of a predetermined number of the data signal lines sequentially connected to each of the video signal lines (4 lines, i.e. S1-S4 to V1, S4-S8 to V2, ... S4(n-3)-S4(n) to Vn, are shown sequentially connected to each video signal line in Fig 1), whose number is the same as the number of the video signal lines (Fig 1 shows n video signal lines and n groups of data lines), said data signal line groups being regarded as a single block (data signal line groups 1-n are "gathered" that is treated as a single block as shown in Figs 4-7, 9, and 10).

Regarding **Claim 21**, *Sunao* teaches a display device, comprising: a display panel (paragraph 0105 and Figs. 13 and 14) which includes (i) a plurality of data signal lines ("S1-S4n" in Fig 1 and paragraph 0025), (ii) a plurality of scanning signal lines provided so as to cross the data signal lines (G1 to Gm in Fig 1 and paragraph 25), and (iii) pixels provided on intersections of the data signal lines and the scanning signal lines (118 in Fig 1 and paragraph 0025), a video signal for displaying an image being fetched from the data signal lines into the pixels in synchronism with a scanning signal supplied from the scanning signal lines (Figs. 1 and 4 and paragraph 0033), said video signal being retained (paragraph 0036 describes "a picture signal...written in a pixel"); a data signal line driving circuit for outputting the video signal to the data signal lines in synchronism with a predetermined timing signal (Figs. 1 and 4 and paragraph 0036); and a scanning signal line driving circuit for outputting the scanning signal to the scanning signal lines in synchronism with a predetermined timing signal (Figs. 1 and 4 and paragraph 0033), said video signal being multiphased ("V1-Vn" in Figs 4-7, 9, and 10), and being supplied to the data signal lines via a plurality of video signal lines ("V1-Vn" in Fig 1 and paragraph 0025 as modified by Fig 12 and paragraph 0101), wherein the data signal line driving circuit, which drives a plurality of data signal lines respectively so as to (a) multiphase the video signal having a plurality of color signals and (b) fetch the video signal into the data signal lines, includes: a plurality of divisional video signal lines, divided so as to respectively correspond to the color signals, which constitute each of the

video signal lines ("V1-Vn" in Fig 1 and paragraph 0025 as modified by Fig 12 and paragraph 0101) ; and a video signal fetching section (Fig 1 sampling circuit 130, switch 131, decoder 140 and sampling signals X1...X4 with operation described in Figs 4-7, 9 and 10 expanded to color by Fig 12 and paragraph 0101) for fetching the video signal from the video signal lines into the data signal lines in each block when gathering data signal line groups (all n data signal line groups are "gathered" that is treated as a single block as shown in Figs 4-7, 9, and 10), each made up of a predetermined number of the data signal lines sequentially connected to each of the divisional video signal lines so as to respectively correspond to the color signals (4 data signal lines, i.e. S1-S4 to V1, S4-S8 to V2, ... S4(n-3)-S4(n) to Vn, are shown sequentially connected to each video signal line in Fig 1 and Fig 12 and paragraph 0101 extend this to color signals), whose number is the same as the number of the video signal lines (Fig 1 shows n video signal lines and n groups of data lines. Fig 12 and paragraph 0101 extend this to color), said data signal line group being regarded as a single block (data signal line groups 1-n are "gathered" that is treated as a single block as shown in Figs 4-7, 9, and 10 and Fig 12 and paragraph 0101 extend this to color).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. **Claims 5, 6, 8, 9, 13, 14, 16, 17, 20, and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over published Japanese Patent Application No. *JP2000-181394* ("*Sunao*") in view of applicants admitted prior art ("*APArt*") and *U.S. Patent No. 5781171 ("Kihara")*.

As to **claims 5 and 6**, *Sunao* discloses the use of shift registers to generate timing signals very similar to those used for fetching video signals. Referring to Fig 4 of Sunao see the similarities between the timing pulses X1 and X2 that cause the video signals to be fetched from the video signal lines to the data signal lines and the signals G1 and G2 for the generation of which Sunao teaches the use of shift registers. Sunao further discloses drive switching means switches between the first driving and the second driving so that the number of

the shift resisters [sic] that operate is varied in switching between the first driving and the second driving and further stopping operation of the shift resister [*sic*] which is not required in driving after switching the drive switching means between the first driving and the second driving. (See paragraph 0014 in which is the teaching to "..stop that part and power consumption" referring to a shift register stage that is not needed because of a reduction in the number of required outputs when a lower resolution driving mode is selected.)

Sunao does not expressly disclose a video signal fetching section that includes one or more shift resisters [*sic*] for generating a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines since Sunao limits specific mention of shift registers to generating scan line timing signals.

APArt discloses a video signal fetching section that includes one or more shift resisters [*sic*] for generating a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines. See for example Figure 22.

Sunao and *APArt* are analogous art because they are from the same field of endeavor, which is video display and seek to solve the same problem, which is to reduce power consumption when switching from display of higher to lower-resolution video signals.

At the time of invention, it would have been obvious to a person of ordinary skilled in the art to modify *Sunao* according to the well known practice of

using shift registers to generate a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines and to include means to vary the number of shift registers used and even stop the operation of unneeded shift registers according to the resolution as taught by *Sunao*. The suggestion/motivation would have been that given by *Sunao*, which is to lower the power consumption (see Abstract and paragraph 0014).

Claims 8, 13 and 16 parallel Claim 5, substituting the word "circuit" for "means" in the cases of Claims 8 and 16, and are rejected using the same arguments (see arguments for Claims 5 and 6 above).

Claims 9, 14 and 17 parallel Claim 6, substituting the word "circuit" for "means" in the cases of Claims 9 and 17, and are rejected using the same arguments (see arguments for Claims 5 and 6 above).

As to **claims 20 and 22**, *Sunao* discloses display devices as set forth in claims 19 and 21.

Sunao does not expressly disclose the data signal line driving circuit, the scanning signal line driving circuit, and the pixels formed on the same substrate.

Kihara discloses the data signal line driving circuit, the scanning signal line driving circuit, and the pixels formed on the same substrate (see Fig. 1 and paragraphs at column 6 lines 31-34 and column 11 line 62 to column 12 line 5).

Sunao and *Kihara* are analogous art because they are from the same field of endeavor, which is display drive.

At the time of invention, it would have been obvious to a person of ordinary skilled in the art to modify the device described in *Sunao* such that the data signal line driving circuit, the scanning signal line driving circuit, and the pixels are formed on the same substrate as taught by *Kihara*. The suggestion/motivation would have been to reduce cost. *Kihara* does not provide motivation directly for the integrated structure but refers to it as the "so-called driver integrated structure" (see column 6, line 32) implying that this type of structure is one of well known value. Since integrating multiple devices onto a single substrate is a well know way to reduce cost, one of ordinary skill in the art at the time of the invention would have recognized its value.

Claim Objections

6. **Claims 15, 16, 17, and 18** are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. **Claims 15, 16, and 17** repeat the limitations of claims 12, 13, and 14 from which they depend. The limitations of **Claim 18** are all recited within Claim 11. Please clarify how the

limitations cited in Claim 18 differ from those cited in Claim 11. Appropriate correction is required.

7. **Claims 1, 2, 3, 4, 5, 6, 8, 9, 10, 11, 13, 14, 16, 17, 18, 19 and 21** are objected to because of the following informalities:

In **Claims 1, 2, 3, 11, 19 and 21** The antecedent of "whose" in the phrase "whose number is the same as the number of the video signal lines" is unclear. It could refer back to "data signal line groups" in the phrase "gathering data signal line groups" whether directly or by referring to "each", or to "data signal lines" in the phrase "of the data signal lines". In the first case the meaning would be that the number of data signal line groups to be regarded as a single block is the same as the number of video signal lines. In the second case the meaning would be that the number of data signal lines (the predetermined number) sequentially connected to each of the video lines is the same as the number of video signal lines. Even though paragraph 0095 of the specification uses the phrase "the data signal line groups whose number is the same as the number of the video signal lines constitute a single block" both meanings are consistent with the specification. Therefore, rewrite the claim to clearly indicate the intended meaning, i.e. "the number of data signal line groups gathered to be regarded as a single block is the same as the number of video signal lines" or change "whose" to "said" to indicate that the "predetermined number" is the same as the number of video signal lines. Appropriate correction is required.

In **Claim 4** the two driving modes (i,ii) as described are equivalent because "each" used as a pronoun means "Every single one of two or more people, animals or things.", (from the AND Concise Dictionary through AllWords.com). Thus the description of (i) becomes "first driving in which every single one of the data signal lines of one of the data signal line groups in the block and every single one of the data signal lines of another one of the data signal line groups in the block are driven at the same time", which is clearly equivalent to (ii). Appropriate correction is required.

In **Claims 10 and 18** equating "data signal line groups" with "data signal line sets" adds no patentable weight to the claim. Either remove the phrase "are data signal line sets" or clarify the distinction between a "data signal line group" and a "data signal line set". Appropriate correction is required.

In **Claims 11 and 21** the phrase "said data signal line group" lacks antecedent basis within the claim. Please clarify the claim language. Appropriate correction is required.

Claims 5, 6, 8, 9, 13, 14, 16, and 17 use the phrase "shift resisters", which is not a recognized term within the art. All references to "shift resisters" in the claims need to be changed to a recognized term such as "shift registers". Note that changing the terminology in the claim will also require changing the terminology in the specification in order to maintain consistent term usage. Appropriate correction is required.

Drawings

8. Figures 11, 20, 21, 22, 23, 24, and 25 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- U.S. Patent 6,229,513 B1 to *Nakano et al.* discloses a reordering unit that produces the interlaced sequence shown in Maeda Fig. 10 (c). See *Nakano* Fig. 5B with n=2.
- U.S. Patent Application 2003/0174117 A1 to *Crossland et al.* with priority to PCT/GB99/024274 discloses reconfigurable shift registers and the use of same to enable an adjacent odd and even row simultaneously (paragraph 0132).

- EP 0 821 338 A2 – *Kay et al.* discloses a configurable panel drive that allows pixels to be driven individually or as multi-pixel groups such that (P5C1L13-16) during reduced resolution operation, the pixels are addressed by contiguous columns and/or rows so as to form the rectangular groups effectively operating as single pixels.

10. Examiner's Notes:

A. It seems that Claim 4 should depend from Claim 1 rather than from Claim 3; Claim 12 should depend from Claim 2 rather than from Claim 11; and Claim 15 should depend from Claim 11 rather than from Claim 14.

B. For the text of *Sunao* I relied on a machine translation from the JPO web site. A copy of this translation is attached.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert R. Rainey whose telephone number is (571) 270-3313. The examiner can normally be reached on Monday through Friday 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Derrick Ferris can be reached on (571) 272-3123. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RR/

7/7/2007

DERRICK W. FERRIS
PRIMARY PATENT EXAMINER